## REMARKS

A Request for Continued Examination (RCE) is being filed concurrently herewith to further prosecute this application.

Claims 1, 3-8 and 17-23 are pending in this application. Independent claims 1, 22 and 23 have been amended hereby to even more clearly recite features of the present invention. Support for the amendments to the claims can be found, for example, in paragraphs [0058] and [0060] of the specification. For the reasons stated below, Applicant respectfully submits that all claims in this case are in condition for allowance.

In the Final Office Action mailed February 23, 2004, all of the claims were rejected over the prior art of U.S. Patent 4,005,454 to Froloff et al., U.S. Patent 5,888,850 to Havens et al., and at least one of U.S. Patent 4,920,574 to Yamamoto et al., Applicant's admitted Prior Art, U.S. Patent 4,994,412 to Kalfus et al., or U.S. Patent 4,980,568 to Merrick et al. These several art-based claim rejections are respectfully traversed.

The present invention is directed to a unique method of making a semiconductor device in which (according to amended claim 1) a semiconductor chip is mounted on a lower conductor with a first solder material applied between the chip and the lower conductor, and an upper conductor is positioned on the chip with a second solder material applied between the chip and the upper conductor. This assembly, with both first and second solder materials, is then placed in a furnace whereby the first and second solder materials are simultaneously heated beyond their respective melting points such that the first and the second solder materials are simultaneously in

a molten state. The device is then removed from the furnace and the first and second solder materials are allowed to solidify. As the first solder material has a melting temperature higher than that of the second solder material, the first solder material is caused to solidify earlier than the second solder material during the solidifying step. This unique method enables the semiconductor chip to be secured on a die pad portion of the lower conductor before the upper conductor is fixedly connected to the semiconductor chip. See amended claim 1 and paragraph [0058] of the specification.

Claims 22 and 23 recite a similar methodology, but specifically recite the use of separate heaters to simultaneously melt the first and second solder materials.

From a reading of the amended claims, it is absolutely clear that the presently claimed invention requires a series of steps in which a semiconductor chip is sandwiched between upper and lower conductors with solder material and that both of these solder materials are simultaneously melted and subsequently allowed to cool and solidify, but at different times, because either the solder material itself is different, or heating is controlled to manage the timing of solidification.

In the "Response to Arguments" of the Final Office Action mailed February 23, 2004, the Examiner takes the position that the combined device or method (combination of Froloff et al., and Havens et al.) shows heating up the first and second solder materials beyond melting points of the respective solder materials, and solidifying the first and the second solder materials, and wherein the first solder material has a melting temperature higher than that of the second solder

material and is caused to solidify earlier than the second solder material in the solidifying step (Havens et al, col. 8, line 55 col. 9, line 5).

Applicant takes exception to the application of the cited prior art.

As already pointed out in previous Responses, it is an important feature for the invention of Havens et al. for reflowing (melting) only the conductors 6 used for connection to an external substrate while holding the conductors 5 in a stable state for keeping intact the required precise electrical coupling between the semiconductor chip 4 and the substrate 3, as clearly described at lines 59-64 of col. 8 referred to by the Examiner himself. In other words, Havens et al. prohibit melting of the conductors 5 (first solder material) when melting the conductors 6 (second solder material). Thus, combining Havens et al. with Froloff et al. in a manner suggested by the Examiner to arrive at the method of the present invention is directly opposite to the teaching of Havens et al.

Again, the presently claimed invention (even before the instant claim amendment, but now emphasized by the amendment) requires a method step in which both the first and the second solder materials are simultaneously molten. Since Havens et al. require that conductors 5 "will be stable" while solder conductors 6 are allowed to reflow, Havens et al. actually teaches the exact opposite to the claimed invention.

Applicant respectfully points out that the Examiner may be confusing a device claim with a method claim. In a device claim, the mere fact that the conductors 5 and the conductors 6 have different melting points may be important. In a method claim, however, the sequence of melting and solidifying the conductors 5 and the conductors 6 is also important. According to the present

invention, the first solder material and the second solder material are melted together by heating up the first and the second solder materials beyond the melting points of the respective solder materials, but the first solder material having a higher melting point is caused to solidify earlier than the second solder material having a lower melting point. According to Havens et al., the conductors 6 alone are melted and solidified while the conductors 5 are kept solid, and this is the critical feature of Havens et al. Apparently, the conductors 6 are deposited onto the substrate 3 after the conductors 5 are melted and solidified for connecting the semiconductor chip 4 to the substrate 3.

Since Havens et al. and Froloff et al. fail to disclose or to suggest the specific method steps recited in the claims now pending in this application, Applicant respectfully requests that the §103 rejections of the claims be withdrawn.

In view of the foregoing all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone applicant's undersigned representative at the number listed below.

SHAW PITTMAN LLP
1650 Tysons Boulevard
McLean, VA 22102
Tel: 703/770-7900

Respectfully submitted,

YOSHITAKA HORIE

Date: October 19, 2004

By: Lawrence D. Eisen (41,009)
for Michael D. Bednarek
Registration No. 32,329

Attachments:

MDB/LDE/ggb

Customer No. 28970